IDEC Chip Design Contest

A High-power-density WR-3.4 Power Amplifier in 250-nm InP DHBT Technology

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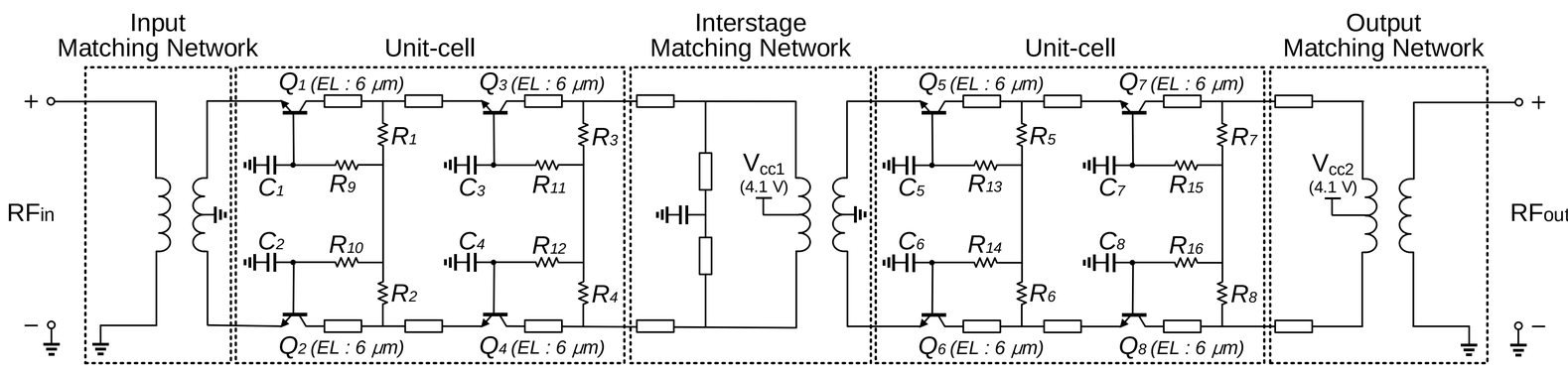
Introduction

- **Advantages of the sub-THz spectrum:**
  - Wide frequency range for the application of ultra-high-speed wireless communication systems
  - Suitable for various applications such as radar, imaging systems, and optical signal processing
- **High-Power Density Power Amplifier (PA) Requirements:**
  - Compact chip area with high output power for phased array systems
  - Low-loss and wideband power combining structures for enhanced output power

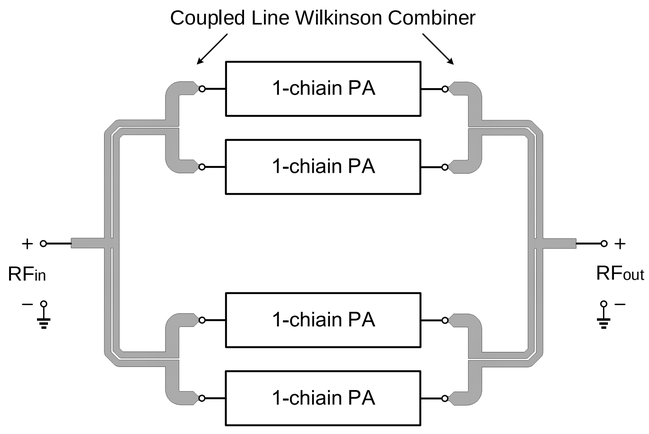
Design

- **1-chain common-base (CB) PA**
  - High-power differential double-stacked CB unit-cell
  - Emitter length selection based on DC power consumption and impedance transformation ratio
  - Impedance matching based on transformer network, transmission lines, and stubs
- **High output power 4-chain CB PA**
  - Four 1-chain CB PAs combined using a coupled-line Wilkinson combiner
  - Using the odd and even-mode characteristic impedances of coupled-line for impedance matching
  - Enhanced output power with efficient combining

(Schematic of the 1-chain CB PA)

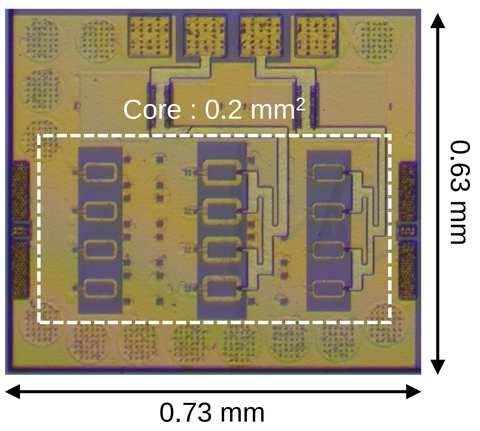


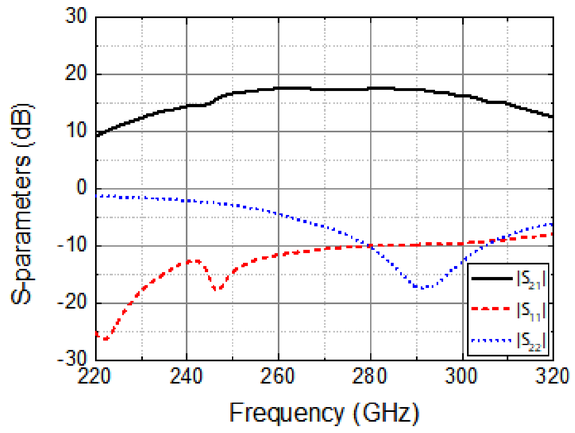
(Diagram of the 4-chain CB PA)

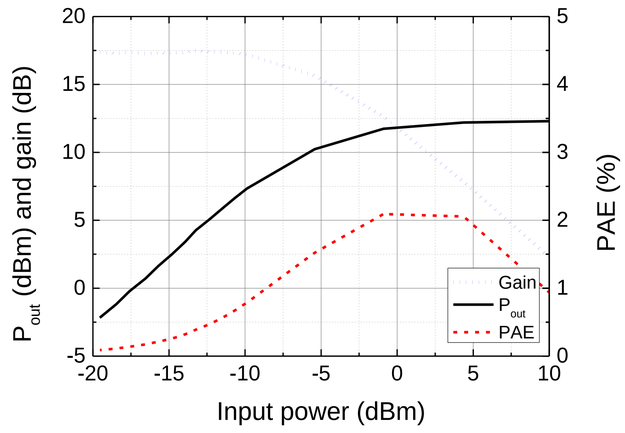


Results

- **Chip photograph & simulated S-parameters**
  - Chip size = 0.73 × 0.63 mm² (Core size = 0.2 mm²)
  - Peak $|S_{21}|$ = 17.5 dB @ 282 GHz
  - 3-dB BW = 69 GHz (243–312 GHz)
- **Measured power performances @ 270 GHz**
  - P_{sat} = 12.4 dBm
  - Peak PAE = 2.0 %
  - Power density = 86.9 mW/mm²







Conclusion

- Design of a high-power-density WR-3.4 power amplifier using 250-nm InP DHBT process
- 4-way coupled-line Wilkinson combiner structure utilized for matching, resulting in a compact chip size
- Achieved P_{sat} of 12.4 dBm with a power density of 86.9 mW/mm²

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea

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